WHAT IS CLAIMED IS:

1. A system comprising:

a logic design module operational to be used by one or more users in logic design tasks; and

a central database integrated with the logic design module and including signal parameters that are accessible to use by the users of the logic design module in the logic design tasks.

2. The system of claim 1 wherein:

the central database includes modifications to the signal parameters, and

the logic design module is structured and arranged to generate a logic design and to update the logic design automatically based on the modifications to the signal parameters in the central database.

3. The system of claim 2 wherein the logic design module is structured and arranged to indicate design discrepancies automatically in the logic design resulting from the modifications to the signal parameters in the central database.

4. The system of claim 3 wherein the indicated design discrepancies include a bit width error.

5. The system of claim 1 wherein the signal parameters include a signal bit width and a value for the signal bit width.

6. The system of claim 1 wherein the signal parameters include a signal bit position and a value for the signal bit position.

7. A method comprising:

defining a signal parameter with a value;

maintaining the defined signal parameter in a central database; and

using the defined signal parameter that is maintained in the central database in computer code for a logic design.

8. The method of claim 7 further comprising:

updating the value of the defined signal parameter in the central database; and

automatically updating the logic design with the updated value of the defined signal parameter.

9. The method of claim 8 further comprising automatically indicating design discrepancies occurring in the logic design that result from updating the value of the defined signal parameter.

10. The method of claim 9 wherein automatically indicating design discrepancies occurring in the logic design includes graphically indicating a bit width error.

11. The method of claim 7 wherein the signal parameter includes a signal bit width and the value includes a value for the signal bit width.

12. The method of claim 7 wherein the signal parameter includes a signal bit position and the value includes a value for the signal bit position.

13. The method of claim 7 wherein the signal parameter includes a bit field and the value includes a value for the bit field.

14. The method of claim 7 further comprising accessing the central database by one or more users.

15. An apparatus comprising:

a central database accessible by one or more users;

one or more signal parameters defined in the central database;

a value for the signal parameters; and

an interface between the central databases and a logic design module that uses the signal parameters in a logic design.

16. The apparatus of claim 15 wherein the signal parameters include a signal bit width and the value includes a value for the signal bit width.

17. The apparatus of claim 15 wherein the signal parameters include a signal bit position and the value includes a value for the signal bit position.

18. A machine-accessible medium, which when accessed results in a machine performing operations comprising:

defining a signal parameter with a value;

maintaining the defined signal parameter in a central database; and

using the defined signal parameter that is maintained in the central database in computer code for a logic design.

19. The machine-accessible medium of claim 18 further comprising:

updating the value of the defined signal parameter; and

automatically updating the logic design with the updated value of the defined signal parameter.

20. The machine-accessible medium of claim 19 further comprising automatically indicating design discrepancies occurring in the logic design that result from updating the value of the defined signal parameter.

21. The machine-accessible medium of claim 20 wherein automatically indicating design discrepancies occurring in the logic design includes graphically indicating a bit width error.

22. The machine-accessible medium of claim 18 wherein the signal parameter includes a signal bit width and the value includes a value for the signal bit width.

23. The machine-accessible medium of claim 18 wherein the signal parameter includes a signal bit position and the value includes a value for the signal bit position.

24. The machine-accessible medium of claim 18 wherein the signal parameter includes a bit field and the value includes a value for the bit field.

25. The machine-accessible medium of claim 18 further comprising permitting one or more users to access the central database.